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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Howard C. Kirsch	Attorney Docket No.: 501048.04
Patent No.	: US 6,812,799 B2	
Issued	: November 2, 2004	
Title	: SYNCHRONOUS MIRROR DELAY (SMD) CIRCUIT AND METHOD INCLUDING A RING OSCILLATOR FOR TIMING COARSE AND FINE DELAY INTERVALS	

NOTIFICATION OF ERRORS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following errors were noted in a review of the above-identified letters patent. One or more of these errors was inadvertently made in the original application, while the others occurred in the printing of the patent. Since the errors are of an obvious nature, a formal Certificate of Correction is not believed to be warranted at this time. Therefore, applicant requests that this notification be placed in the Patent and Trademark Office file.

Column, Line	Reads	Should Read
Item (56), Other Publications, Jang Reference	"Jang, Seong-Jin et al. A Compact Ring Delay Line for High Speed Synchronous DRAM, IEEE Symposium on VLSI Circuits Digest of	--Jang, Seong-Jin et al. "A Compact Ring Delay Line for High Speed Synchronous DRAM," IEEE Symposium on VLSI Circuits Digest of

	Technical Papers, 1998, pp. 60-61.	Technical Papers, 1998, pp. 60-61.--
Item (56), Other Publications, Takai Reference	"Takai, Yasuhiro et al., A 250 Mb/s/pin 1Gb Double Date Rate SDRAM wtih a Bi-Directional Delay and an Inter-Bank Shared Redundancy Scheme, 1999."	--Takai, Yasuhiro et al., "A 250 Mb/s/pin 1Gb Double Date Rate SDRAM with a Bi-Directional Delay and an Inter-Bank Shared Redundancy Scheme," 1999.--
Column 1, Line 9	"is now a U.S. Pat. No."	--is now U.S. Pat. No.--
Column 2, Line 27	"unit delays **11**A-N"	--unit delays **110**A-N--
Column 3, Line 3	"DFDCLK signal"	--the DFDCLK signal--
Column 6, Line 15	"Once skilled in the art"	--One skilled in the art--
Column 6, Line 32	"response to rising edge"	--response to a rising edge--
Column 8, Line 29	"of latch and compare"	--of the latch and compare--
Column 9, Line 36	"that place the"	--that places the--
Column 9, Line 55	"with a low or frequency"	--with a lower frequency--
Column 10, Line 17	"T**3** , may not be used"	--T**3,** may not be used--
Column 10, Line 41	"signals in the SM**1**"	--signals in the SMD--
Column 11, Line 5	"that is to be output"	--is to be output--
Column 11, Line 45	"Columns **3** indicates the ending value of the down count"	--Column **3** indicates the ending value the down count--
Column 11, Line 48	"zero –1 in some cases"	--zero to –1 in some cases--
Column 12, Line 19	"in response to a rising edged"	--in response to a rising edge--
Column 12, Line 48	"When ever the CEN signal"	--Whenever the CEN signal--
Column 12, Line 62	"having rising and the falling"	--having rising and falling--
Column 13, Line 20	"edges of the CLK signal"	--edges of the CLK signal.--
Column 14, Line 48	"provides two 32 bits"	--provides two 32 bit--

Column 14, Line 57	"received N/2 bits words"	--received N/2 bit words--
Column 16, Line 13	"such as output devices"	--such output devices--
Column 16, Line 25	"may be made in detail, and yet"	--may be made in detail and yet--
.Column 17, Line 56	"oscillator clocks signals,"	--oscillator clock signals,--
Column 23, Line 32	"claim **37** Wherein"	--claim **37** wherein--

Respectfully submitted,

Date: July 31, 2006

By: _____

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Enclosure:
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